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HEPHY INSTITUT FÜR HOCHENERGIEPHYSIK

Projektarbeit

Determining TJ-Monopix2 parameters and behavior at different temperatures for Belle II VTX Upgrade

Im Rahmen des Studiums

Technische Physik

unter der Betreuung von

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1 Background

1.1 Introduction

The quest to understand reality's nature, dating back to Democritus's theory of fundamental building blocks, has culminated in the standard model of particle physics, thanks to a series of discoveries and technological advancements. The evolution of detectors, crucial to advance in nuclear and particle physics, has undergone significant transformations. From the discovery of radioactivity and the invention of the cloud and bubble chambers, which allowed particle visualization, to the development of fully electronic readout systems like the multi-wire proportional chamber, detector technology has continually evolved to meet the demands of modern experiments.

These experiments necessitate the detection of numerous particle tracks with micrometer spatial resolution and nanosecond timing accuracy. The invention of the transistor and advancements in silicon microelectronics marked a significant leap in detector technology. Following Moore's law, the miniaturization of electronic devices has progressed exponentially, leading to the manufacture of position-sensitive segmented detectors with micro-structured electrodes. Silicon microstrip detectors, developed in the 1980s, continue to be used today due to their high channel densities and spatial resolution.

Pixel detectors, the next stage in this evolution, offer 3D space points crucial for pattern recognition, tracking, and reconstructing vertices of short-lived particles. They combine a low material budget with high channel densities, with each pixel functioning as an independent smart sensing element. This integration level, made possible by modern sub-μm CMOS processes, allows pixel detectors to handle high interaction rates and energies, essential for probing increasingly rare processes.

1.2 Physics Motivation

The standard model of particle physics accurately describes subatomic particle interactions, encompassing three of the four fundamental forces. Nevertheless, it leaves unanswered questions, notably the matter-antimatter asymmetry. Andrei Sakharov identified prerequisites for this imbalance, including baryon number violation and charge (C) and parity (CP) asymmetry. While CP violation was initially observed in kaon decays and later explained through three-generation quark mixing, it falls short in explaining the universe's baryon density. Addressing such gaps, research seeks 'New Physics' beyond the standard model. Three strategies dominate:

- **High-Energy Particle Collisions:** Focused on detecting new particle manifestations, CERN's LHC is at the forefront. Its most notable achievement is the discovery of the Higgs boson. ATLAS and CMS experiments at CERN explore properties of the Higgs and potential new particles, considering theories like Supersymmetry.
- **Precision Measurements at Lower Energies:** New heavy particles can affect lower-energy processes, marking deviations from the standard model. The Belle experiment at KEK lab, Japan, exemplifies this approach. It found CP violation in B meson decays, supporting the quark mixing theory. Its successor, Belle II, amplifies this research with substantially more data to refine understanding of new physics.
- **Non-Accellerator based experiments:** Certain particles can not be generated by current collider technology, and have therefore be detected "in the field". These particle types include astro-particles and rare events like neutrino collisions, or other subjects like dark matter.

2 The Belle II experiment

2.1 The superKEKB collider

The KEK Super B Factory (**Fig. 1**) located at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, represents a significant advancement in the field of particle physics [5]. This facility is designed to provide unparalleled insights into the interactions and behaviors of subatomic particles. The primary objective of the Super B Factory is to achieve high luminosity and precision measurements, making it an essential tool for researchers worldwide.

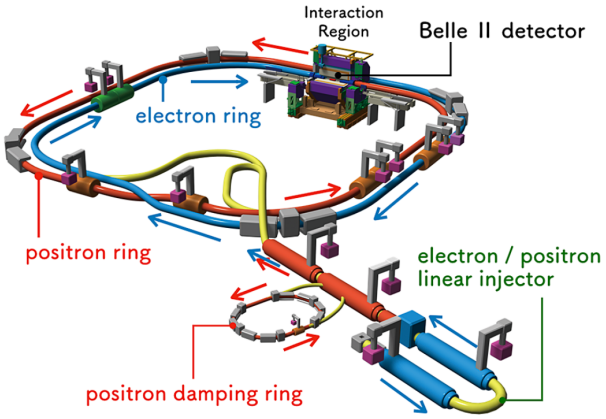

Fig. 1: Schematic drawing of SuperKEKB/Belle II facility [6]

2.2 The current Belle II vertex detector

The Belle II Detector (**Fig. 2**)[4], is a state-of-the-art instrument designed for precision measurements in particle physics and is part of the superKEKB collider. Its primary purpose is to study B-meson decays, which are crucial for understanding the differences between matter and antimatter. The design of the Belle II detector largely follows the design of its predecessor [11], with modifications to accommodate the "nano-beam" collider and the larger crossing angle.

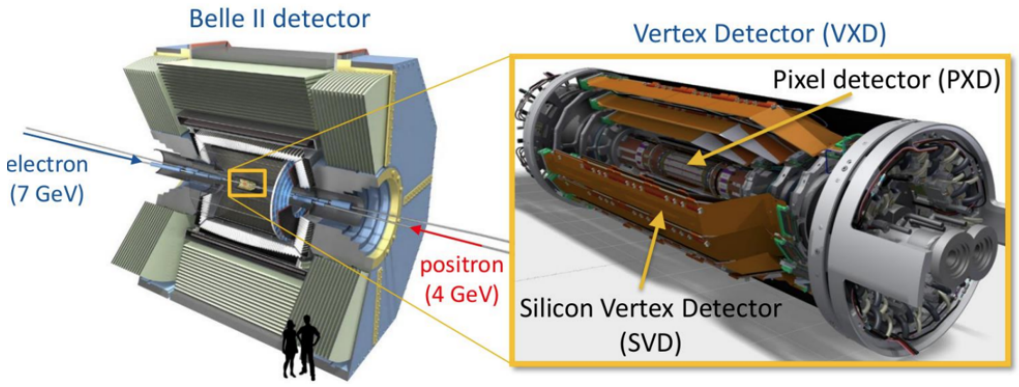

Fig. 2: Belle II detector [1]

2.2.1 Pixel Detector (PXD)

The Pixel Detector of Belle II is optimized for precision vertex reconstruction of B-meson decays. The DEPFET sensors used in the pixel detector are monolithic all-silicon sensors without the need for additional support and cooling material in the active region of the detector. These

sensors are thinned to 75 μm. Positioned close to the beam at 14 mm, the PXD faces an extremely high luminosity, nearing $6x10^{35}cm^{-2}s^{-1}$. Such luminosity conditions result in a surge of background particles, background rate and considerable radiation damage. To address this, the detector features a fine granularity with a pixel size of 50 μm x 50 μm and a high readout rate of 50 kHz, limiting the background occupancy to 1-2%.

2.2.2 Silicon Vertex Detector (SVD)

The Belle II Silicon Vertex Detector consists of four layers of double-sided silicon detectors made from six-inch wafers. These layers are located at radii of 38, 80, 115, and 140 mm from the beam pipe, positioned between the Pixel detector and the Central Drift Chamber. The SVD uses the APV25 readout chip with a shaping time of 50 ns. This, combined with online hit time reconstruction at a precision of 2-4 ns, ensures a low occupancy rate. The front-end modules of the SVD are cooled by CO2.

2.3 Vertex Detector (VXD/VTX)

The combination of both PXD and SVD sensors is called Vertex Detector (VXD). The current VXD of Belle II is approaching its capacity limits, with significant uncertainties. Given this, the Belle II team is contemplating introducing an enhanced VXD system by 2027 to ensure safety against the projected background and potentially improve tracking and vertexing capabilities. The VTX group is in the initial stages of crafting a pixelated VXD, termed VTX, leveraging rapid and detailed Depleted Monolithic Active Pixel Sensors (DMAPS) on lightweight supports. This DMAPS combines both the sensor and the front end electronics onto the same chip. A standout feature of the VTX design is its uniform sensor type across all layers and a material allocation under 2% radiation length, in contrast to the existing VXD's two sensor technologies and roughly 3% radiation length.

2.4 VTX-Upgrade

For the planned upgrade, a new DMAPS, OBELIX, tailored specifically for Belle II's unique requirements, is being developed, building upon the TJ-Monopix2 DMAPS. [2]
Shown in **Fig. 3** is a rendering of the new VTX layout, showing the five layers of Sensors around the collision chamber.

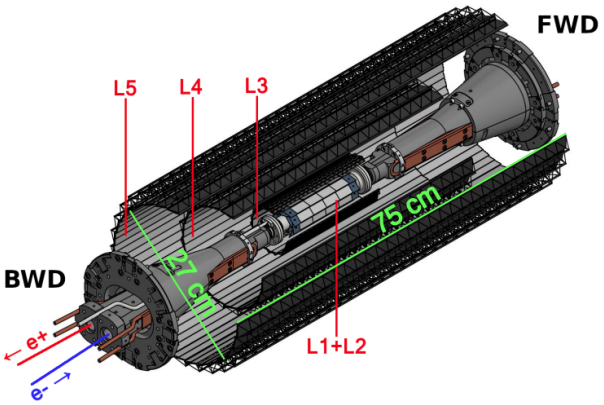

Fig. 3: VTX CAD rendering [2]

The new sensor will run at a lower clockrate and has about 20% larger pixels. The reduced clockrate leads to a lower power consumption, which will be further reduced by optimizing certain operational parameters, which is one of the main objectives of this project.

3 TJ-Monopix2

The TJ-Monopix2 chip (**Fig. 4**) is characterized by its high resolution and excellent sensitivity, making it suitable for a wide range of applications, including scientific research, medical imaging, and industrial inspection. The chip is designed to provide high-quality images with low noise and high dynamic range. It was originally developed for the ATLAS experiment using the TowerJazz 180nm CMOS process[3]. This process has been in use for almost a decade in high energy physics, with the most recent addition being the ALPIDE chips used in the ALICE experiment at CERN. It allows for high-density pixel arrays and low power consumption. The pixel size is 33 x 33 μm^2, and the chip contains 512 x 512 pixels. The chip also includes several advanced features, such as in-pixel amplification and digitization, which improve the quality and make the chip more versatile. The chip also supports a high frame rate, allowing for fast image capture and processing.

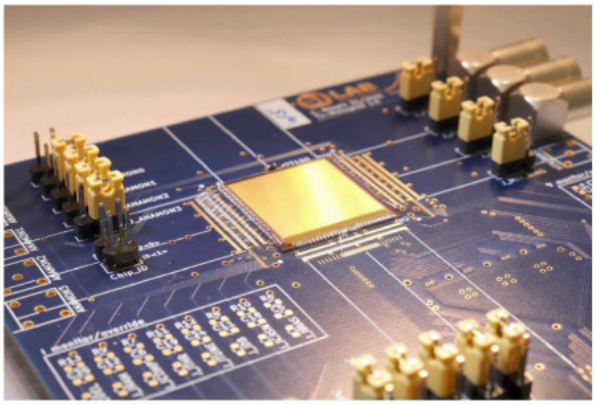

Fig. 4: TJ-Monopix2 sensor on breakout board [1]

3.1 Analysis of High Chip Failure Ratio

In this section, we delve into the comprehensive investigation conducted to address the issue of the high chip failure ratio. The hypothesis suggests that during the wire bonding process, certain pads might have been unintentionally damaged, resulting in possible shorts and a detrimental impact on the chip's overall performance. To gain a deeper understanding of the situation, the bonding wires were deliberately removed, and the chip was cut along the right pads, as depicted in the images below (**Fig. 5**).

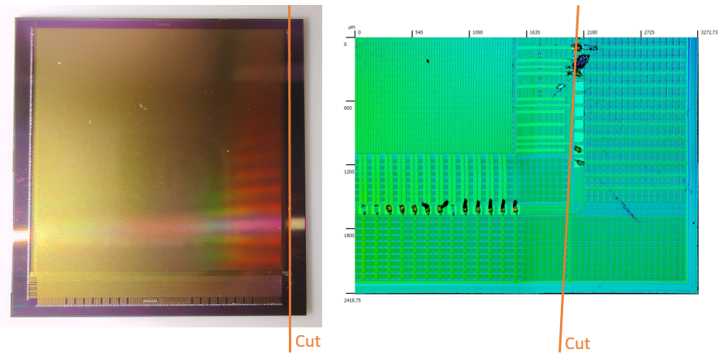

Fig. 5: Illustration of cutline through TJ-Monopix2

3.2 Investigation of Chip Structure and Pad Defects

The TJ-Monopix2, features a pad pitch of 120μm. Understanding the chip's construction and identifying any anomalies are crucial steps in ensuring its reliability and optimal performance. Fig. 6 seen on the left provides a close up view of the TJ-Monopix2 chip pad pitch, while Fig. 7 seen on the right shows a functional Pad. These SEM pictures were kindly recorded by technicians at the TU Vienna by first cutting the sample along the previously marked line, and then analyzing the samples in the FEI Quanta 250 FEG [10].

Fig. 6: TJ-Monopix2 pad pitch overview

Fig. 7: Functional pad

3.2.1 Damaged biasing pad

This pad was subjected to a more detailed investigation because of erroneous power readings in the biasing circuit. The most notable finding is a gap between Layer one and two of the pad, which is filled with a foreign substance (**Fig. 8**).

Fig. 8: SEM Picture of the damaged biasing pad

3.2.2 Damaged grounding pad

Several significant observations were made during the examination.

- **Gap between Layers:** A noticeable gap was observed between the first and last two layers of the pad. This gap can affect the electrical connectivity of the pad and may lead to performance issues.
- **Foreign Material:** The gap mentioned above was found to be filled with particles of a foreign material. The presence of this can hinder proper contact and lead to reduced functionality.
- **Bonding Foot Stuck on the Pad:** An additional issue was identified, where the bonding foot got stuck on the pad and could not be removed without further damaging the Chip.

Fig 9 illustrates the observed defects. The magnified upper cutout shows the stuck bonding Foot. The magnified lower cutout shows the damaged layer structure of the Pad.

Fig. 9: SEM picture of the damaged grounding pad whit magnified cutouts

3.3 Conclusion: Analysis of damaged Pads and posibile causes

The current hypothesis regarding the damaged pads is damage due to too much stress on the substrate during the bonding process, likely an effect of too high bonding energy. This stress causes the internal layers to separate slightly, leading to higher than wanted internal resistances, or, if a layer breaks completely, internal short circuits. Evidence for this theory is the stuck bonding foot which couldn't be removed without further damaging the Chip and presence of what is presumably grinding dust between the layers in the SEM images. This dust was likely introduced during the preparation of the chip for the SEM, and could only make its way between the layers of the chip if there was previous damage to that area.

To address these challenges and improve chip integrity, our next step involves bonding a chip with lower bonding energy. By reducing the bonding energy, we aim to mitigate layer damage and enhance the chip's long-term performance.

4 Tuning the system parameters

The TJ-Monopix2 is split into four different sectors (**Fig. 10**) [8]: The Normal Front End (N-FE), the normal cascode frontend (NC-FE), the high voltage front end (HV-FE) and the high voltage cascode front End (HVC-FE). The cascode frontends contain an additional transistor to increase gain, while the HV frontends have a special AC-coupled design. Only the behavior of the first 16 columns of each the normal and normal cascode frontend was analyzed.

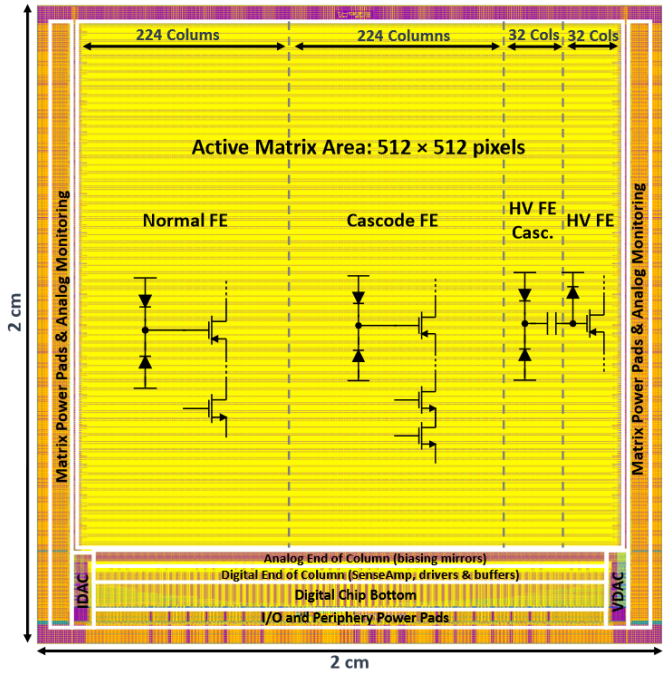

Fig. 10: Physical layout of the TJ-Monopix2 [8]

4.1 Test setup and used components

The TJ-Monopix2 was connected to the PC running the measurement scripts using a BDAQ53 board [12]. This board features a Kintex-7 FPGA, and connects to the chip's breakout board via two DisplayPort cables. The communication between BDAQ and the PC was established via Ethernet.

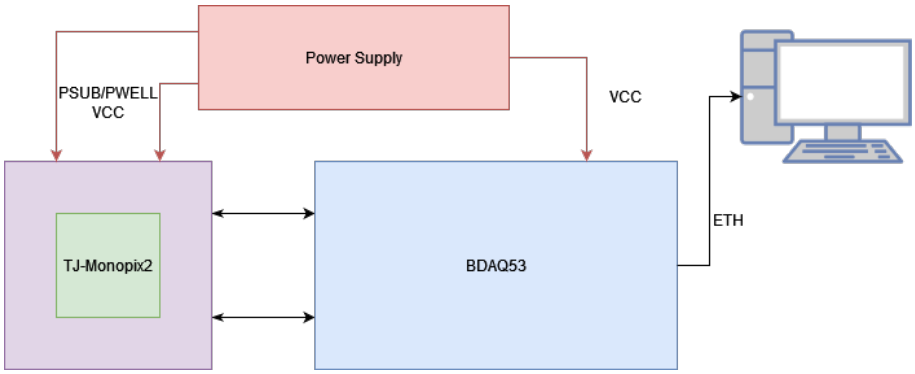

Fig. 11: Test setup

On the software side, python scripts with specialized libraries [9] were used to control the chip during measurement sequences and to change various register parameters.

4.2 Description of Measurements

The focus was on Chip W8R19 (Wafer 8, Reticle 19) with the objective of achieving a target threshold of 28 DAC units. A DAC unit describes the relative sensitivity of each pixel to an external influence. Setting this value too high would result in high noise figures, while lower values reduce the overall sensitivity of the readout. New global and local tunings were applied for each setting, and values were recorded after both global and local tuning processes. The global tuning process attempts to roughly optimize the performance of the entire Chip, while the local tuning takes each pixel into account individually to produce a more precise result.

4.2.1 Power Consumption

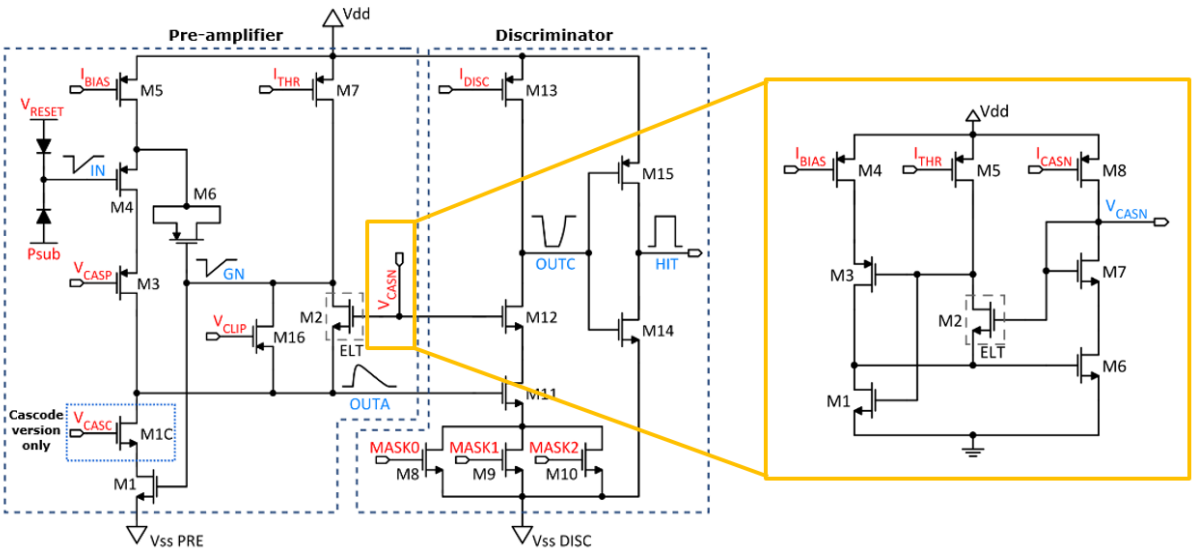

Fig. 12: Schematic of the TJ-Monopix2 frontend circuit [8]

Throughout the experiments, the following register settings were varied:

- IBIAS ranged from 100 to 50 with a step size of 10
- ITHR ranged from 65 to 30 with a step size of 5
- IDB ranged from 100 to 50 with a step size of 10
- VCASC ranged from 248 to 218 with a step size of 10

Lower values in these registers correspond to a lower overall power draw. IBIAS, ITHR and IDB control the current available to the chip in different areas of the frontend. VCASN adjusts the pre-amplifier output baseline. The points of impact of these register settings can be seen in Fig. 12. These variations allowed for a comprehensive assessment and optimization of this chip's power consumption compared to performance.

4.2.2 Timewalk

The timewalk describes the delay in ns from injecting a charge of a certain intensity into the chip to the signal being transmitted. It is measured by injecting a charge of a known intensity into the chip at a certain point in time, and then measuring how long the chip takes to respond.

4.3 Normal Front End

4.3.1 IBIAS Variation

The results are presented in the Fig. 13. During this investigation, the other two parameters, ITHR and IDB, were left at their standard values.

The first column shows the variation of the ICASN register compared to IBIAS. The second cloumn shows the mean threshold (μ_{TH}), the third column shows the standard deviation (σ_{TH}) and the last column shows the mean noise threshold (μ_{noise}). For all the diagrams with two lines, one line describes the "untuned" results (only global tuning) and the other line showes the "tuned" result (including local tuning).

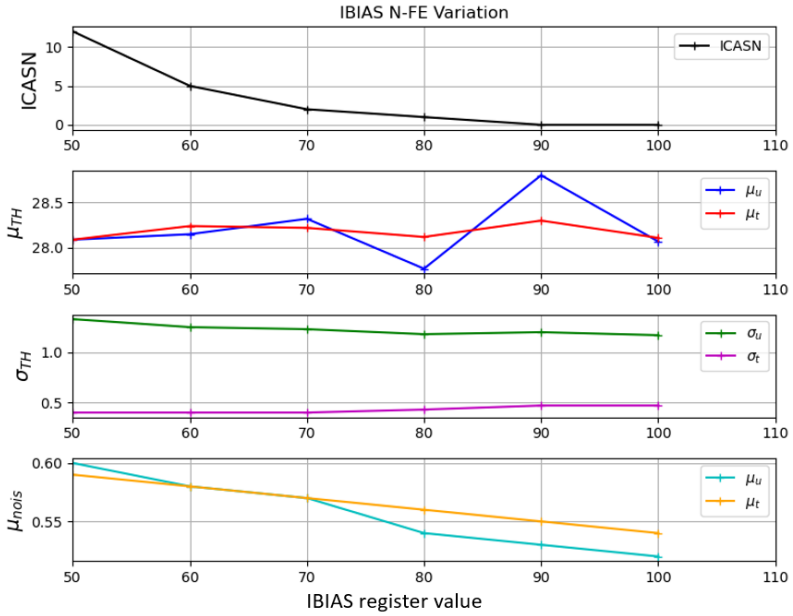

Fig. 13: IBIAS variation N-FE

Analyzing the graphs allows the following conclusions.

- The global tuning of ICASN effectively counters the effects of IBIAS reduction. This tuning process played a crucial role in keeping the performance of the N-FE within acceptable ranges, despite the changes in IBIAS.
- The local tuning process was successful overall, even though the results with only global tuning started drifting.
- With changing IBIAS there was a slight change in the noise distribution. This change warrants further investigation to ensure that the overall noise levels remain within the desired specifications.

Fig 14 illustrates the timewalk for different IBIAS settings in the Normal frontend configuration. All values were recorded from a single pixel to eliminate other factors.

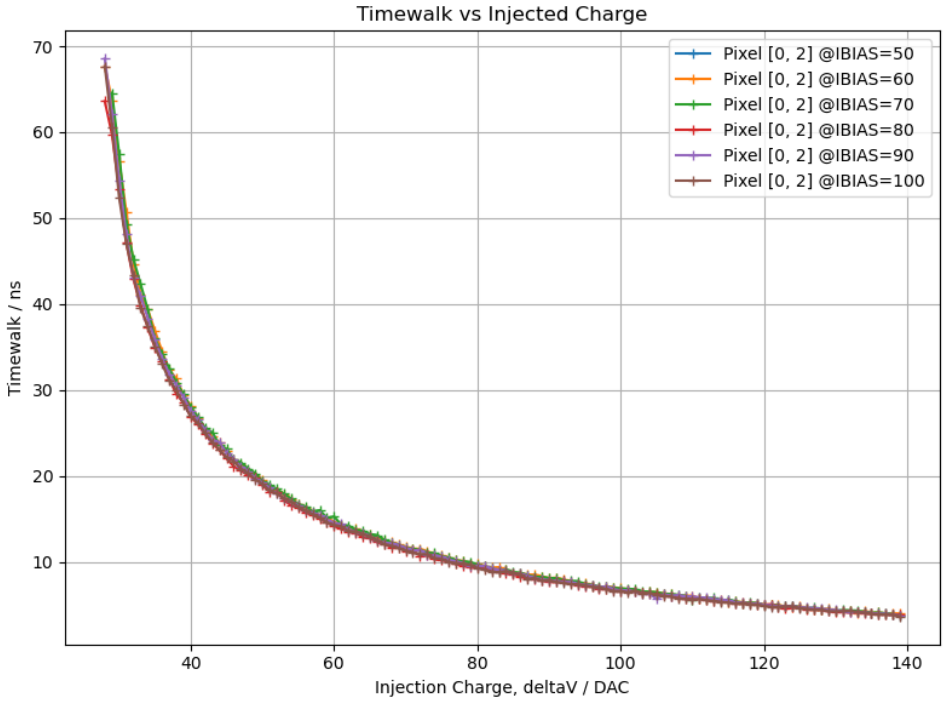

Fig. 14: IBIAS timewalk N-FE

- **Timewalk Analysis:** The timewalk is a critical parameter affecting the chip's performance. Surprisingly, no obvious changes between setups could be observed. This indicates that the timewalk remains stable despite changes in IBIAS values.
- **Y-Axis Offset:** It is important to note that there is a slight offset on the Y-axis in the presented figures. This offset is attributed to the system delay and does not affect the overall analysis.

These measurements were repeated in the same way for the remaining registers, so only the outcomes are described, not the whole procedure.

4.3.2 IDB Variation

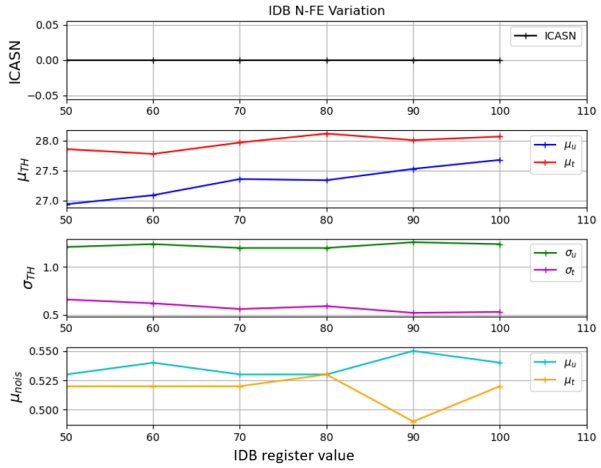

Fig. 15: IDB variation N-FE

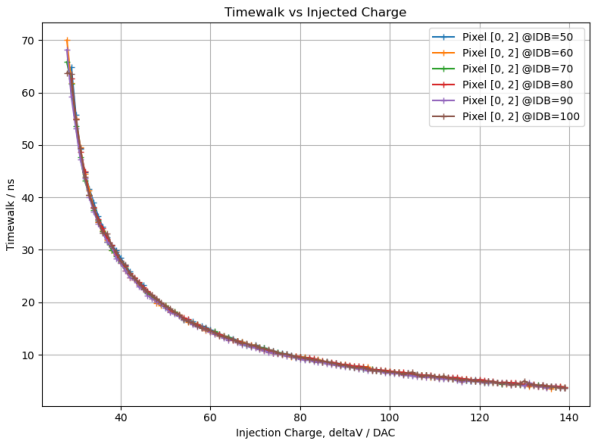

Fig. 16: IDB timewalk N-FE

From the graph above, following conclusions can be drawn:

- ICASN seems to be unaffected by changes in IDB. Any changes in the threshold results were mitigated by the local tuning process. (**Fig. 15**)
- The variation in IDB did not produce any significant changes in the timewalk behavior. (**Fig. 16**)

4.3.3 ITHR Variation

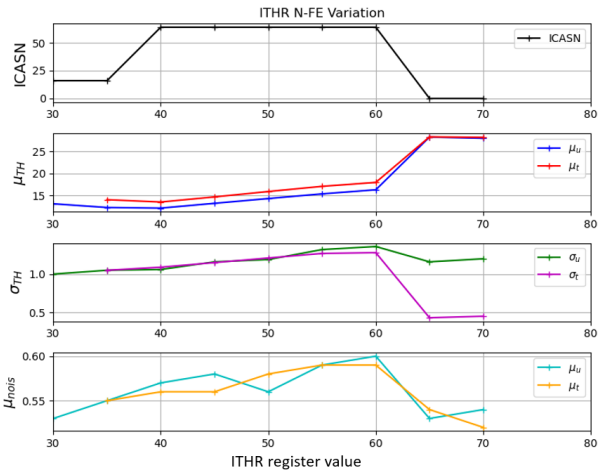

Fig. 17: ITHR variation N-FE

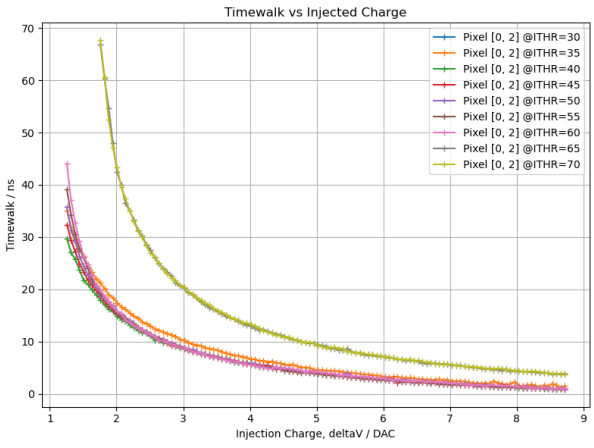

Fig. 18: ITHR timewalk N-FE

As observed in the graph (**Fig. 17, Fig. 18**), we can draw following conclusions:

- As visible in the second diagram, the target threshold of 28 DAC-Units could not be reached with ITHR Values below 65.
- ICASN attempts to compensate for low ITHR Values.
- Relative deviation and noise levels show bad results for ITHR < 65, but stabilize above.
- Due to the strongly shifting threshold values, the timewalk curves also vary greatly.

4.4 Normal Cascode Frontend

4.4.1 IBIAS Variation

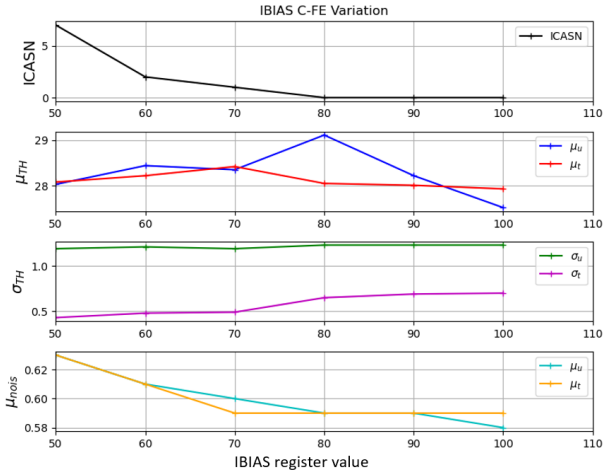

Fig. 19: IBIAS variation C-FE

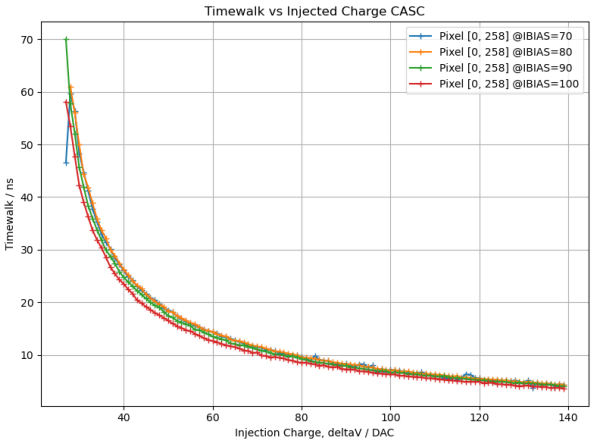

Fig. 20: IBIAS timewalk C-FE

As observed in the graph (**Fig. 19, Fig. 20**), we can draw following conclusions:

- The global tuning of ICASN effectively counters the effects of IBIAS reduction.
- The local tuning process was successful overall, even though the results with only global tuning started drifting.
- With changing IBIAS there was a slight change in the noise distribution.
- With higher IBIAS values, the timewalk improves slightly. The biggest observable difference is about 3ns.

4.4.2 IDB Variation

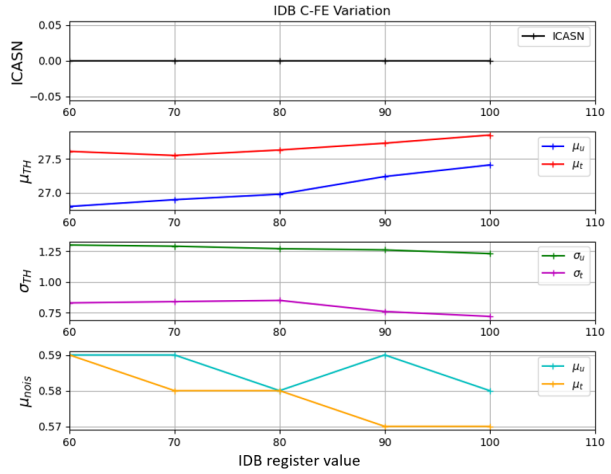

Fig. 21: IDB variation C-FE

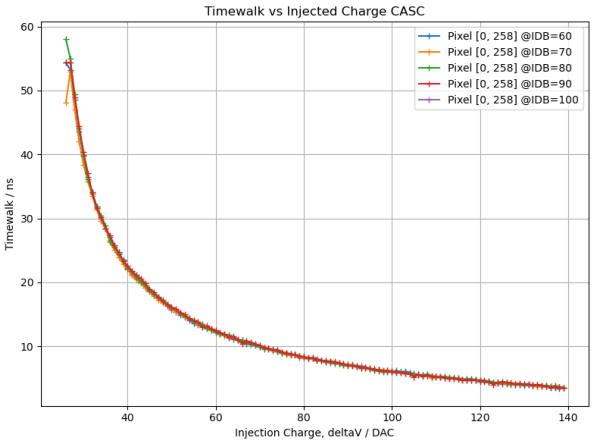

Fig. 22: IDB timewalk C-FE

From the graph above, several conclusions can be drawn:

- ICASN seems to be unaffected by changes in IDB. Any changes in the threshold results were mitigated by the local tuning process. (**Fig. 21**)

- The variation in IDB did not produce any significant changes in the timewalk behavior. (**Fig. 22**)

4.4.3 ITHR Variation

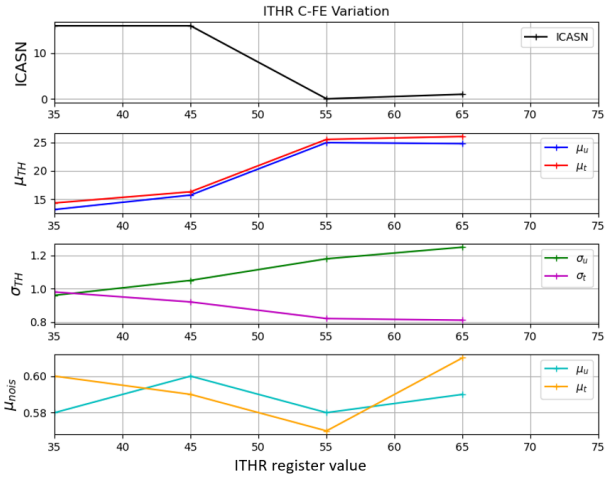

Fig. 23: ITHR variation C-FE

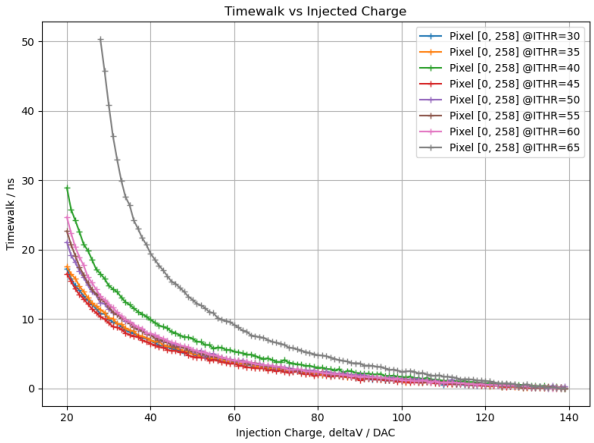

Fig. 24: ITHR timewalk C-FE

As observed in the graph (**Fig. 23, Fig. 24**), we can draw following conclusions:

- As visible in the second diagram, the target threshold of 28 DAC-Units could not be reached with ITHR Values below 55.
- ICASN attempts to compensate for low ITHR Values.
- Relative deviation and noise levels show bad results for ITHR < 55, but stabilize above.
- Due to the strongly shifting threshold values, the timewalk curves also vary greatly.

4.4.4 VCASC Variation

The results are presented in the figure below.

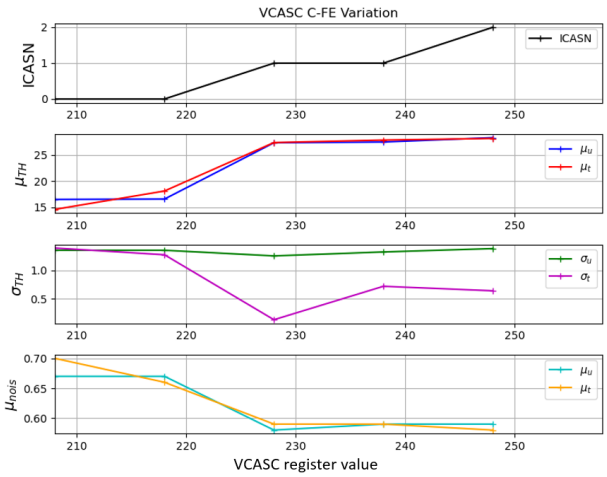

Fig. 25: VCASC variation C-FE

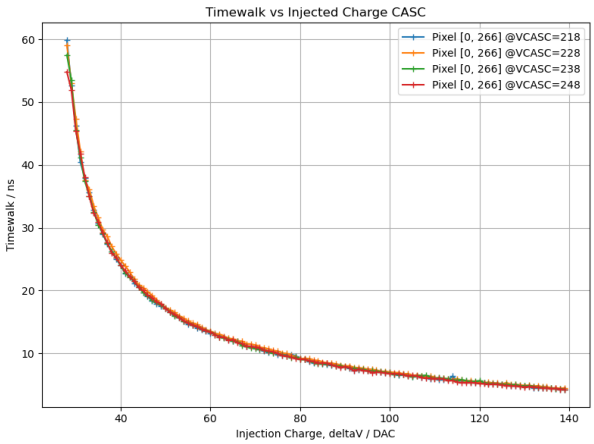

Fig. 26: VCASC timewalk C-FE

As observed in the graph (**Fig. 25, Fig. 26**), we can draw following conclusions:

- Low VCASC settings exhibited lower stability and caused more frequent crashes.
- As visible in the second diagram, the target threshold of 28 DAC-Units could not be reached with VCASC Values below 228.
- Despite the changing threshold, the timewalk remains stable across all values, this indicates the transistor M1C not influences the timewalk.

4.5 Conclusion: Impact of changing the system parameters

IBIAS shows very little influence on either frontend, with only the cascode timewalk varying slightly (3ns). High values tend to have slightly better noise characteristics, though nothing significant. The recommended value here is between 60-70, as it shows relatively low ICASN values, combined with good performance.

IDB has negligible influence on either frontend in all measurements. This value can therefore, unless other interactions occur, be lowered to 50.

ITHR shows the largest impact on the performance of the chip, with lower values decreasing the performance significantly. This value also has a big impact on the timewalk. Therefore, it is not recommended to go below 65, especially if other factors are also being changed.

VCASC shows very stable results above a certain threshold, but bad resolution beneath it. It should not be lowered beneath 228 to avoid negative impacts on measured data.

These results will directly affect the development process of the upcoming OBELIX chip, and help to decrease its power consumption. This should allow for lower operating temperatures even in an air cooled environment, which, as discussed in the next chapter, leads to lower latencies across the chip.

5 Temperature Measurements

This section outlines the parameters measured during the experiment, as well as their corresponding descriptions. The data was collected at various temperatures, ranging from -10°C to 60°C, to understand the performance of the device under different thermal conditions. Only the TJ-Monopix2 was placed in a climber chamber for this purpose. [7]

5.1 Description of Measurements

- **Injection Crosstalk Delay @40MHz:** The measurement of injection crosstalk delay at 40MHz evaluates the interference between injection signals at this frequency and aids in reducing signal distortions. Fig. 27 shows the linear combination of T_{inj} minus the timestamp delay BCID (Bunch Crossing ID) T_{BCID}. It therefore describes the time difference between an injected signal and its associated timestamp.
- **Injection HitOr Delay:** This measurement indicates the maximum delay between the injected signal of an individual pixel and the hit signal leaving the chip. Understanding this delay is essential for optimizing the device's response time, especially in regard to the upcoming OBELIX chip, which features a higher temporal resolution. Fig. 28 shows the linear combination of T_{inj} plus the propagation delay over all OR-gates T_{HitOr}.
- **Injection BCID Delay @IDEL=40:** This measurement focuses on the delay of the injected signal with respect to BCID, specifically when IDELAY (Injection Delay) is set to 40 (approximately 40ns). Fig. 29 shows the linear combination of T_{inj} plus the global delay value in the IDEL register T_{del} minus the timestamp delay T_{BCID}

These measurements each describe a different physical aspect of the chip. The Injection Crosstalk value is the delay inside each column, HitOr describes the propagation delay through the various OR-Gates between colums and injection BCID describes the delay of the entire signal chain.

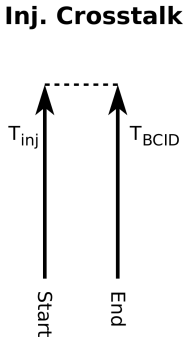

Fig. 27: Crosstalk Delay

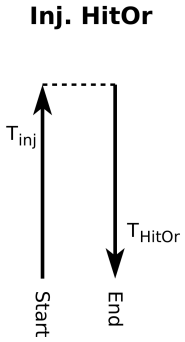

Fig. 28: HitOr Delay

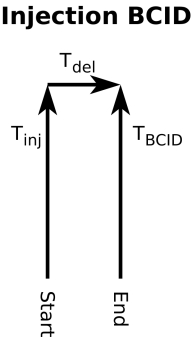

Fig. 29: BCID Delay

Table 1 shows the different linear combinations mathematically.

Measurement	Symbol	Composition			
Injection Crosstalk	$T_1 =$	T_{inj}		$-T_{BCID}$	
Injection HitOr	$T_2 =$	T_{inj}			$+T_{HitOr}$
Injection BCID	$T_3 =$	T_{inj}	$+T_{del}^{40}$	$-T_{BCID}$	

Tab. 1: Different linear combinations

5.2 Used Tuning

Since the chip had to be taken all the way to 60°C, a lower quality sample was used. It was tuned to a threshold of 30 DAC units to ensure stable operation under non temperature controlled conditions. For chip W8R3, only a -2V PSUB/PWELL setting was utilized, which already resulted in a high leakage of approximately 9mA. "Good" samples usually use a bias voltage of around -6V. The tuning was conducted at a stable temperature of 22°C, ensuring that the chip's performance can be evaluated in a controlled environment.

Scan config	Value
VCAL_HIGH	110
VCAL_LOW_start	100
VCAL_LOW_step	-1
VCAL_LOW_stop	65
n_injections	100
start_column	0
start_row	0
stop_column	32
stop_row	512

TJ-Monopix2 config	Value
IBIAS	100
ITHR	64
ICASN	2
IDB	100
ITUNE	170
ICOMP	80
IDEL	88
IRAM	50
VRESET	120
VCASP	93
VCASC	228
VCLIP	255

Fig. 30: Used Tuning

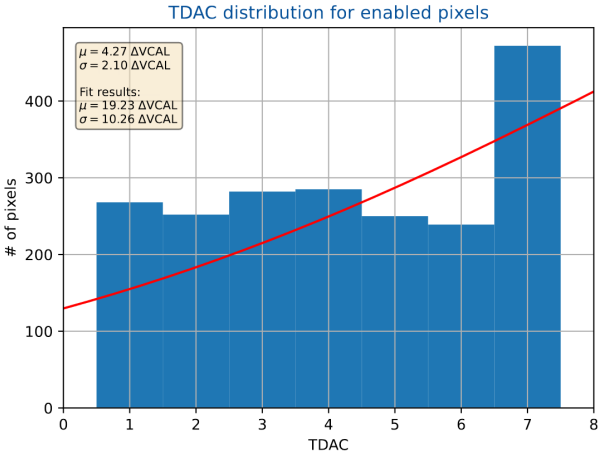

Fig. 31: TDAC distribution

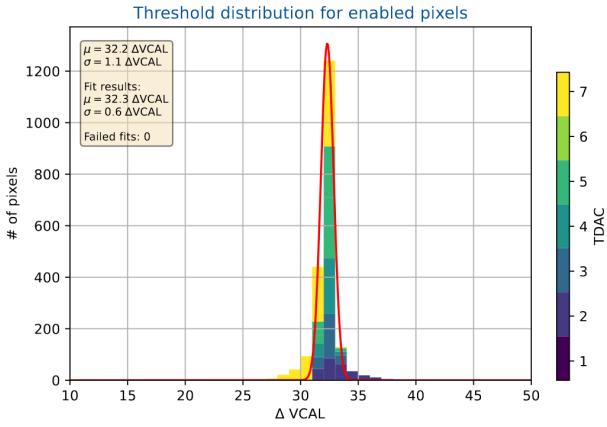

Fig. 32: Threshold distribution

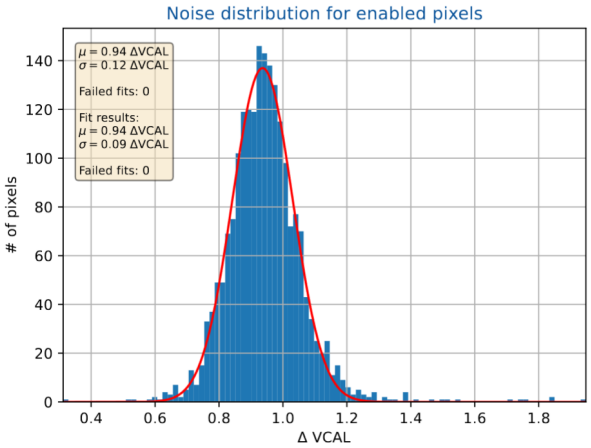

Fig. 33: Nois distribution

Fig. 30 shows the standard register values for all following tests. These values are based on previous simulations and will be refined over time. Fig. 31 image shows how much different pixels have to be compensated with TDAC, a 3-bit value that is specific to each pixel. More extreme values (1&7) mean a higher correction factor. These values are the results of a local tuning procedure conducted beforehand. Fig. 32 shows the normal distribution of the different pixels in regard to a set calibration target. Notably, pixels with a higher TDAC value tend to be on the low side of the target signal, while pixels with a low TDAC can be found further to the right of the graph, showing that the active compensation of each pixel works as intended. Fig. 33 shows a distribution plot of overall pixel noise, to avoid any outliers or erroneous measurements.

5.3 S-Curves at different Temperatures

The S-Curve measurement shows the relation between the pixel noise levels and occupancy levels. This allows the determination of the average threshold and mean deviation.
Fig. 34 - Fig. 40 show that the threshold accuracy in each measurement increases with rising temperatures, up to about 40°C.

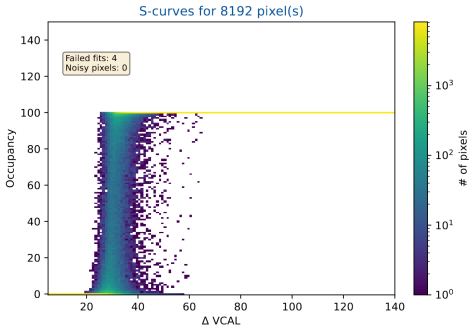

Fig. 34: -10°C

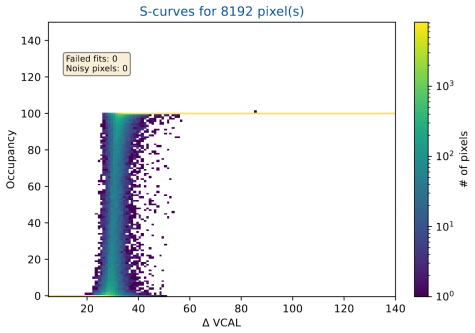

Fig. 35: 0°C

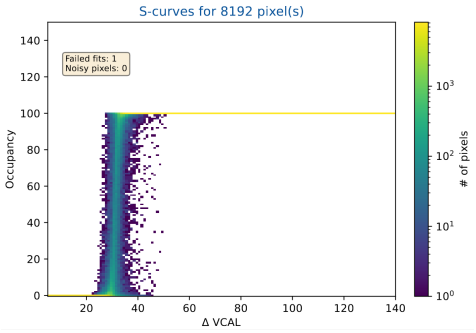

Fig. 36: 10°C

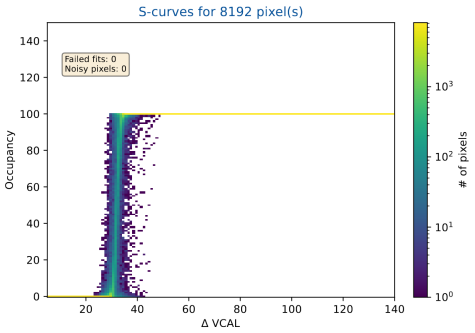

Fig. 37: 20°C

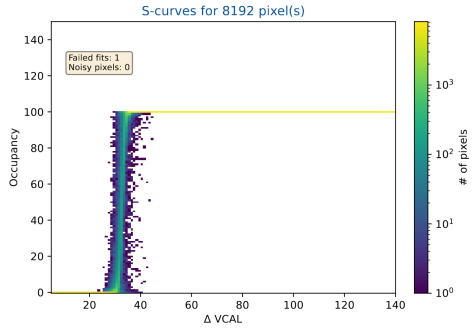

Fig. 38: 30°C

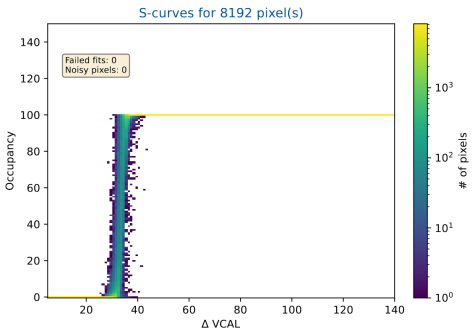

Fig. 39: 40°C

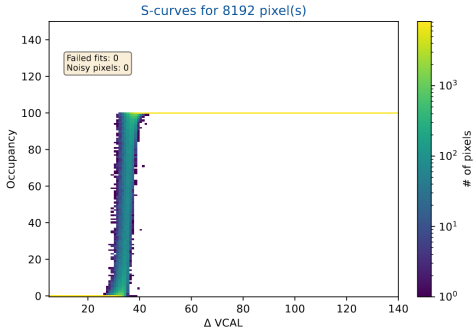

Fig. 40: 60°C

5.4 Threshold Variation at different Temperatures

The graph below (**Fig. 41**) illustrates the relationships between temperature, S-curve mean threshold value (μ) and average dispersion (σ).

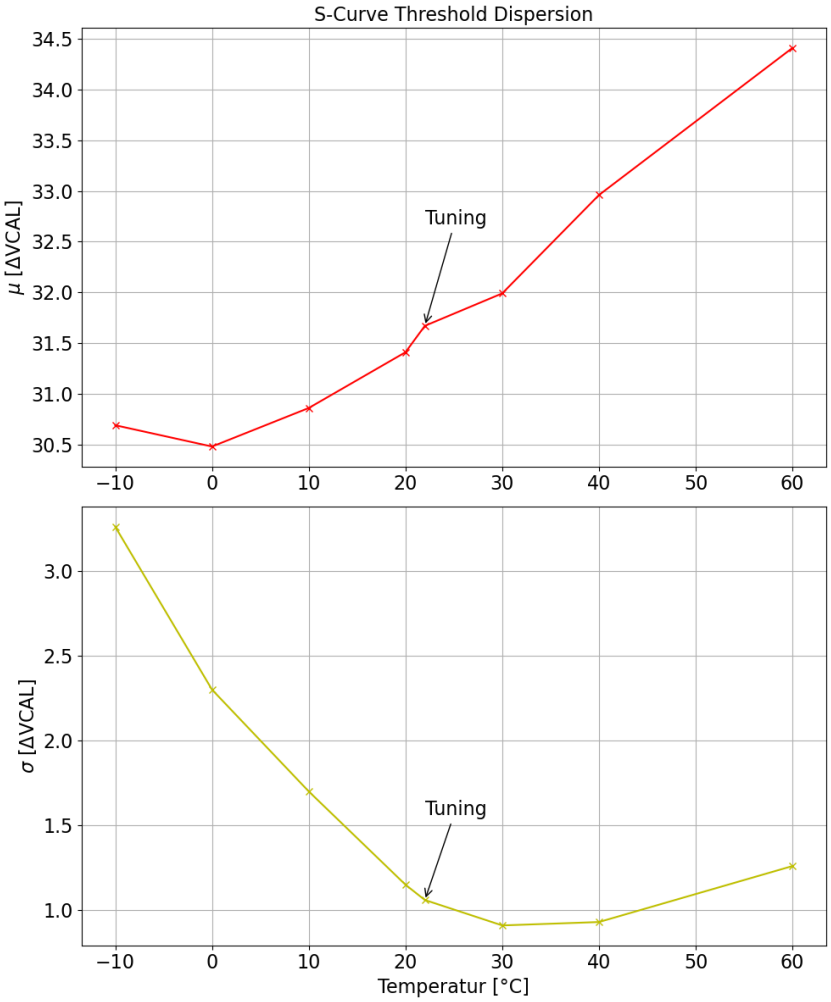

Fig. 41: Threshold dispersion for different temperatures

- **Temperature vs. Mean Threshold:** As the temperature increases, there is a noticeable, yet not drastic, rise in the mean threshold value.
- **Temperature vs. Threshold Dispersion:** The measurements show that the average deviation decreases as temperatures increase. This hints to the chip preferring temperatures slightly above room temperature.
- **Temperature Coefficient of Threshold:** The temperature coefficient of the threshold, which measures ≈ 0.7 DAC-Units/10K, is deemed acceptable for Testbeam applications. This coefficient indicates the sensitivity of the chip's threshold to temperature changes.
- **Retuning at -10°C:** Re-tuning the chip at -10°C slightly improves threshold dispersion. However, this improvement is limited by the TDAC range.

5.5 Maximum HitOr Delay at Different Temperatures

To determine the maximum HitOr injection delay at each temperature, the value was measured by using a linear fit over all rows, and choosing the maximum time. Fig. 42 shows one of these measurement results. From these values, another linear fit was calculated for the overall HitOr max values.

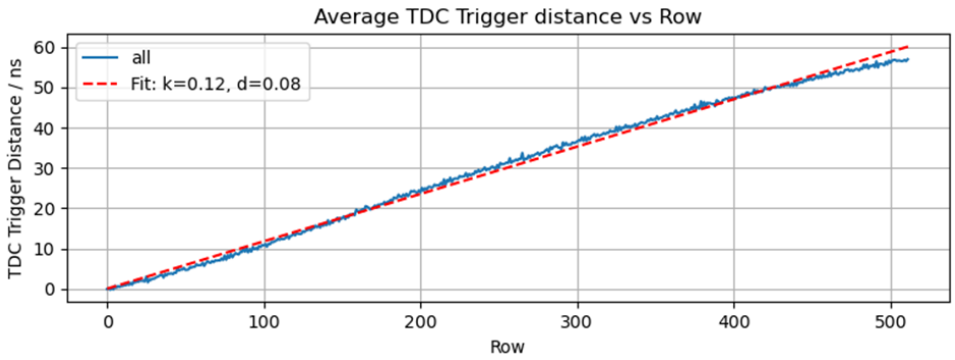

Fig. 42: Average TDC trigger distance vs row at 22°C

Fig. 43 illustrate the relationship between temperature and the maximum HitOr injection delay. As the temperature increases, there is an observable increase in the maximum HitOr injection delay. This data suggests that logic gates slow down with rising temperatures, affecting the overall performance of the chip.

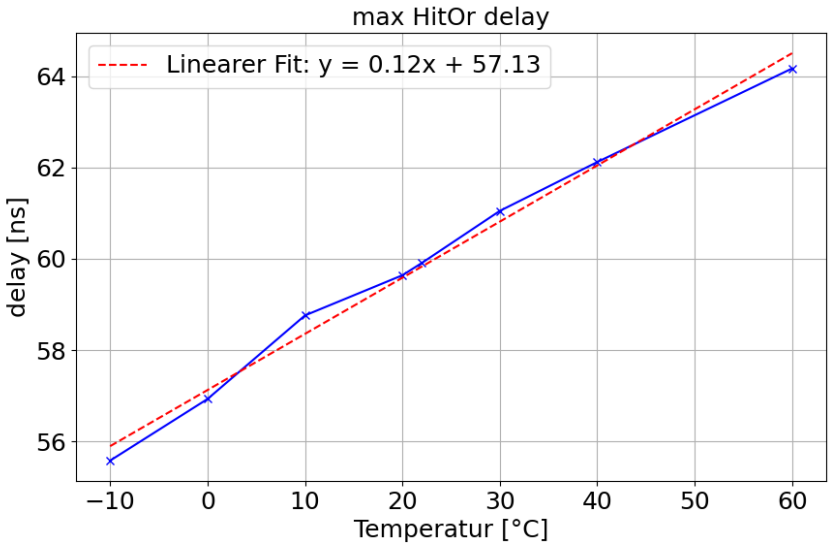

Fig. 43: Maximum HitOr Delay for different temperatures

5.6 Injection BCID delay at different temperatures

Fig. 44 shows the injection delay between the first and last row at different BCIDs at a constant temperature. The important part here is the delta between the activation of row 0 and row 511.

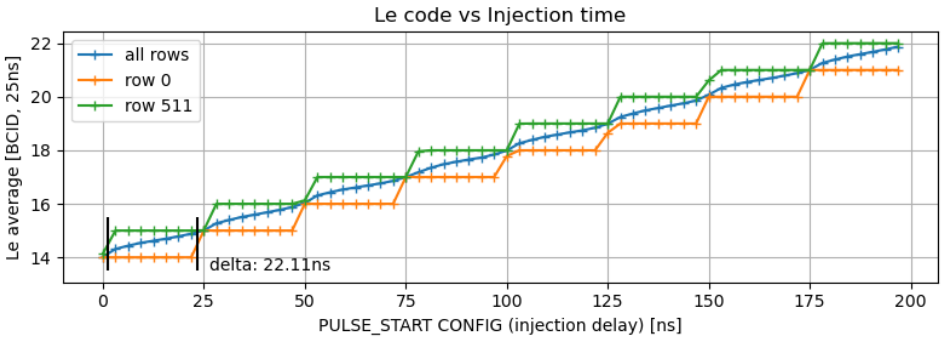

Fig. 44: Injection BCID delay at 22°C

Fig. 45 shows the relationship between the measured BCID delays at different temperatures and different BCIDs. The different lines represent the different BCIDs.

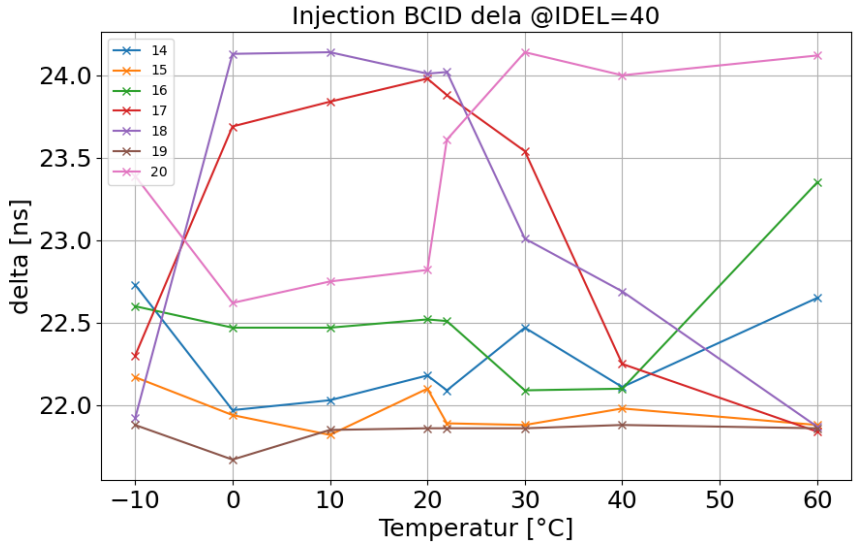

Fig. 45: Injection BCID delay over all temperatures @IDEL=40

The BCID delay results show no change that can be attributed to temperature variation. Any variation between results is most likely due to slight timing inaccuracies in the measurement setup, as the differences observed are often in the sub-nanosecond range. More precise instrumentation would be required to accurately determine any temperature influence.

5.7 Injection Crosstalk delay at different temperatures

In Fig. 46 one can see the measurement strategy for this test. The timing delay between row 0 and row 511 is determined by measuring the time difference between the two low-points of the signals.

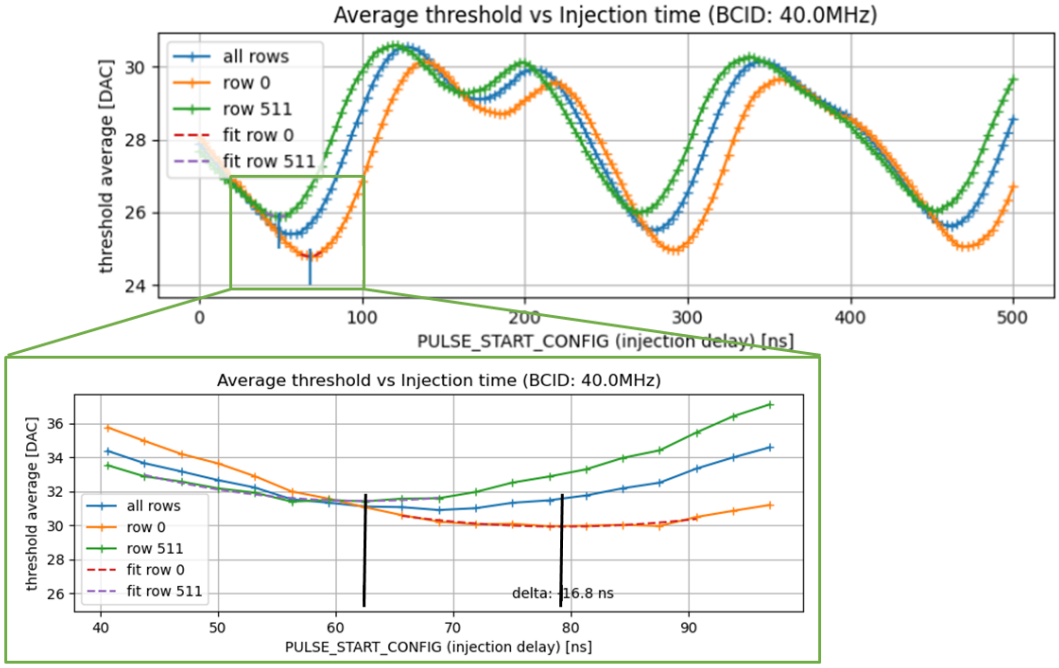

Fig. 46: Average threshold vs injection time at 20°C

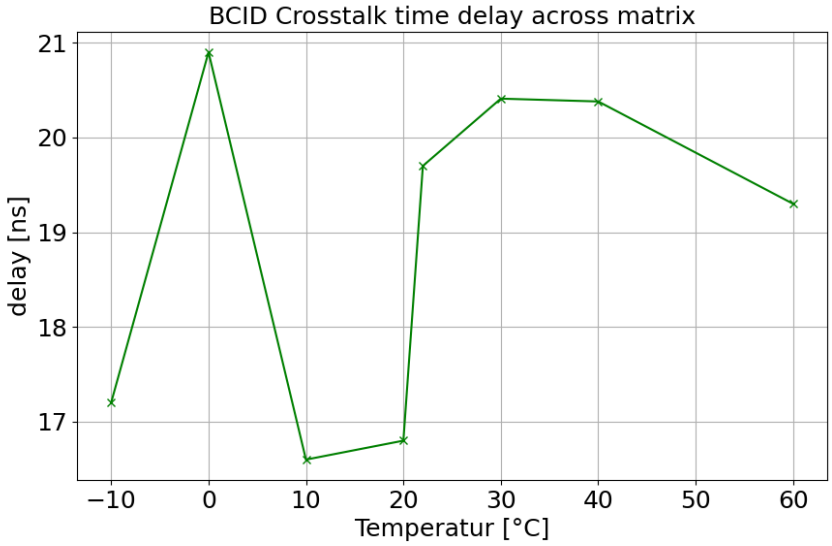

Fig. 47: Injection Crosstalk delay over different temperatures @40MHz

As visible in the diagram (**Fig. 47**), temperature does not seem to have a direct impact on BCID crosstalk delay. Since the chip was not retuned between runs, it is also unlikely that other factors have changed between runs. Therefore, this result is, so far, inconclusive as to what exactly influences the crosstalk delay, and how to control this parameter more precisely.

5.8 Conclusion: Investigating temperature effects on chip performance

- **Effects of varying Temperature:** The chip demonstrates increased variability at lower temperatures, and also a more general offset between different temperature levels. This observation highlights the need to consider temperature effects when designing and operating the chip in diverse environmental conditions.
- **HitOr Delay vs. Temperature:** HitOr delay shows a consistent increase with rising temperature, with a temperature coefficient of approximately 2.33ns/10K. This temperature dependency can impact the chip's response time and overall performance. Therefore, any thermal limits should be set with these limitations in mind.
- **Threshold Variation with Temperature:** The threshold values exhibit an upward trend with increasing temperature. The temperature coefficient of the threshold is observed to be approximately 0.7 DAC-Units/10K. After retuning the chip at -10°C the graph is roughly linear again, meaning these values should be relatively predictable over a wide range of temperatures.
- **Threshold Dispersion:** When tuned at room temperature, the threshold dispersion demonstrates a minimum around 25°C to 40°C. This shows that the chip can be tuned in room temperature environments without compromising on performance while it is in use.
- **Chip Stability:** As the chip stability decreases with extreme temperatures, it is important to define an appropriate temperature envelope for normal operation, and to ensure the device stays within these limits when in use. Since low temperatures lead to frequent connection errors and data loss, a working temperature of >20°C is recommended.
- **Crosstalk and BCID Delay:** Due to the small variations between runs, no accurate correlation between temperature and crosstalk or BCID delays could be found. This indicates that these changes are most likely not noticable during normal operation.

Considering all measured values, a normal operation temperature between 25-40°C Ambient Temperature seems to be the sweet spot for this chip. In future iterations the temporal resolution of BCID measurements should, if possible, also be increased, to avoid the same measurement errors visible in this project work.

6 Overall Conclusion

The results of this work will be used to improve development and deployment of future OBELIX chips and their supporting infrastructure. Importantly, the mounting of future iterations of the chip has to be optimized, so bonding errors and damage on different pads can be avoided. A first step towards this goal would be reducing the bonding energy used, which should put less stress on individual parts of the chip.
Recommended operating parameters for the current iteration of chip are:

- **IBIAS:** This value has very little influence overall, with only the cascode timewalk being influenced slightly. The recommended value is **60-70**
- **IDB:** This value has almost no influence on all measurements. The recommended value is **50**.
- **ITHR:** ITHR shows the largest impact on performance overall, especially on the timewalk. This value should not be set below **65** to avoid major performance degradation.

- **VCASC:** VCASC shows a clear threshold underneath which operation becomes very unstable, whereas above this threshold performance does not change. The recommended value is **228**.
- **Temperature:** Since the HitOr delay of the chip directly depends on the temperature of the chip, overly high operating temperatures should be avoided. Similarly, below a certain temperature, data readout starts to get unreliable, making a minimum operating temperature necessary. The overall best temperature range seems to be between **25-40°C**.

These values will likely have to be refined further for the OBELIX chips, but should provide a good jumping off point to further optimize performance and power consumption/heat dissipation.

List of Tables

List of Figures

References

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